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$Al_{0.44}Ga_{0.56}N$ spacer layer to prevent electron accumulation inside barriers in lattice-matched InAlN/AlGaN/AlN/GaN heterostructures

M. Akazawa,[1,2,a)] B. Gao,[1] T. Hashizume,[1,2] M. Hiroki,[3] S. Yamahata,[3] and N. Shigekawa[3]
[1]*Research Center for Integrated Quantum Electronics, Hokkaido University, Sapporo 060-8628, Japan*
[2]*JST–CREST, Sanbancho, Chiyoda-ku, Tokyo 102-0075, Japan*
[3]*NTT Photonics Laboratories, NTT Corporation, Atsugi, Kanagawa 243-0198, Japan*

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The barrier structure in lattice-matched InAlN/GaN heterostructures with AlGaN-based spacer layers grown by metal organic vapor phase epitaxy was studied by the capacitance-voltage (C-V) method. To investigate the characteristics under positive bias, an Al_2O_3 overlayer was added. The C-V characteristic of a sample with an $Al_{0.38}Ga_{0.62}N$ (5 nm)/AlN (0.75 nm) double spacer layer exhibited an anomalous saturation at a value far below the insulator capacitance under positive bias, which indicated electron accumulation at the InAlN/AlGaN interface. The C-V characteristic of an alternative sample with a single $Al_{0.44}Ga_{0.56}N$ (1.5 nm) spacer layer did not exhibit the anomalous saturation. © *2011 American Institute of Physics*. [doi:10.1063/1.3578449]

A lattice-matched InAlN/GaN heterostructure provides a high-density two-dimensional electron gas (2DEG) due to the difference in spontaneous polarization at the interface without any doping.[1,2] To enhance electron mobility, an AlN ultrathin layer has been used as a conventional spacer layer.[3,4] Several reports have been published on the application of the InAlN/AlN/GaN structure to field-effect transistors (FETs) (Refs. 3–5) including normally off type FETs.[5] A recent study, however, reported that the insertion of an $Al_{0.38}Ga_{0.62}N$/AlN double spacer layer improved surface flatness and electron mobility compared with those for a single AlN spacer layer.[6] Since the band gap of an $Al_{0.38}Ga_{0.62}N$ layer is smaller than that of a lattice-matched InAlN layer, electron accumulation might occur at the InAlN/AlGaN interface under positive bias, resulting in a reduction in the effective barrier thickness. Schottky barrier diodes are not suitable for investigating electron accumulation in the barrier layer under positive bias. One of the methods of clarifying electron accumulation inside the barrier layer is to measure capacitance-voltage (C-V) characteristics using samples with an insulator overlayer on the heterostructure. In this letter, the $Al_{0.38}Ga_{0.62}N$/AlN double spacer layer is reappraised. A sample with an $Al_{0.44}Ga_{0.56}N$ single spacer layer is also investigated as an alternative structure, for preventing electron accumulation inside the barrier layer.

Figure 1 shows the structures of the test samples. An Al_2O_3 (10 nm)/$In_{0.17}Al_{0.83}N$ (10 nm)/$Al_{0.38}Ga_{0.62}N$ (5 nm)/AlN (0.75 nm)/GaN (2 μm) structure and an Al_2O_3 (13 nm)/$In_{0.18}Al_{0.82}N$ (12 nm)/$Al_{0.44}Ga_{0.56}N$ (1.5 nm)/GaN (2 μm) structure were fabricated and tested. The fabrication process of the test samples was as follows. Heterostructures were grown by metal organic vapor phase epitaxy. For the cap-annealing process to form an Ohmic contact, a 20 nm thick SiN_x layer was deposited by electron-cyclotron resonance chemical vapor deposition using a SiH_4/Ar and N_2 gas mixture at 260 °C. After opening a ring-shaped window by lithography and wet etching using buffered hydrofluoric acid (BHF, $HF:NH_4F=1:5$) solution, a ring-shaped Ti/Al/Ti/Au (30 nm/50 nm/20 nm/100 nm) Ohmic electrode was formed. Then the samples were annealed in N_2 ambient at 800 °C for 1 min. After removing the SiN_x layer using BHF solution, an Al_2O_3 overlayer was deposited by atomic layer deposition (ALD) at a substrate temperature of 250 °C. Finally, a circular Ni/Au (20 nm/50 nm) electrode was formed in the center of the Ohmic ring.

The Hall measurement showed that the $In_{0.17}Al_{0.83}N$ (10 nm)/$Al_{0.38}Ga_{0.62}N$ (5 nm)/AlN (0.75 nm)/GaN heterostructure in Fig. 1(a) produced a 2DEG with a sheet carrier density, n_S, of 2.2×10^{13} cm^{-2} and an electron mobility, μ, of 1400 $cm^2/V/s$, reproducing the previously reported results.[6] The obtained C-V characteristic for the Al_2O_3/$In_{0.17}Al_{0.83}N$/$Al_{0.38}Ga_{0.62}N$/AlN/GaN structure is plotted in Fig. 2. A step at approximately 0 V can be seen in the C-V curve in addition to the usual step at approximately −11.5 V, indicating the depletion of the 2DEG. From the capacitance values, the plateau at the negative bias corresponds to electron accumulation at the AlN/GaN interface. Even though the positive bias range was limited due to the leakage through the Al_2O_3 layer, the capacitance step at 0 V tends to saturate at a value much lower than the insulator capacitance, C_i, of approximately 260 pF. The saturation capacitance corresponds to the value for electron accumulation at

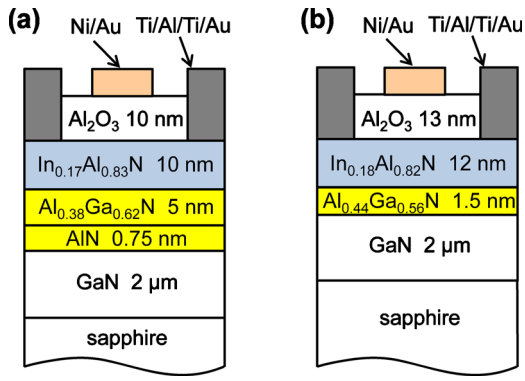

FIG. 1. (Color online) Schematic sample structures.

a)Electronic mail: akazawa@rciqe.hokudai.ac.jp.

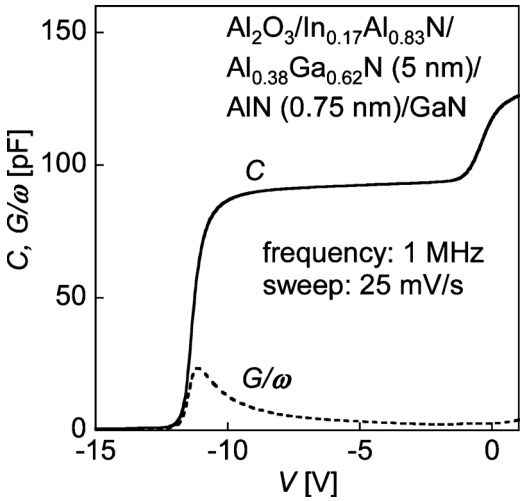

FIG. 2. Measured C-V curve for the Al_2O_3 (10 nm)/$In_{0.17}Al_{0.83}N$ (10 nm)/$Al_{0.38}Ga_{0.62}N$ (5 nm)/AlN (0.75 nm)/GaN structure. C_i was estimated to be ~260 pF. The bias voltage was swept from the positive side to the negative side at a sweep rate of 25 mV/s.

the InAlN/AlGaN interface. This phenomenon may become a drawback of the heterostructure if it is applied to an FET gate, resulting in parallel conduction and a complicated change in potential.

Figure 3 shows conduction band, E_C, potential profiles with respect to the Fermi level, E_F, calculated for the $In_{0.17}Al_{0.83}N/Al_{0.38}Ga_{0.62}N/AlN/GaN$ heterostructure by solving the Poisson and Schrödinger equations self-consistently[7] for several positions of the surface Fermi level, $E_{F\ surf}$. The band alignment based on the amphoteric native-defect model[8] and related experimental data[9,10] was assumed in the calculation, while the interface charge due to polarization was estimated in accordance with Ref. 1. For the sample with an $Al_{0.38}Ga_{0.62}N/AlN$ spacer layer, it can be seen that applying positive bias leads to electron accumulation at the InAlN/AlGaN interface. In the sample with the Al_2O_3 overlayer, electron accumulation at the InAlN/AlGaN interface is expected to occur before that at the $Al_2O_3/InAlN$ interface because E_C for the AlGaN layer is closer to E_F than that for the InAlN layer, which is consistent with the measured C-V curve. The spacer layer should be thinner with a wider band gap to prevent electron accumulation inside the barrier layer.

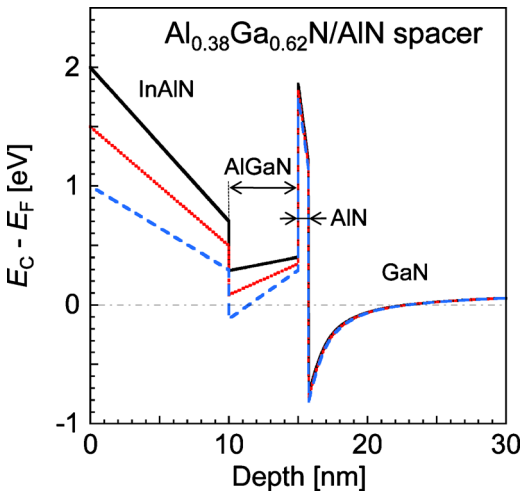

FIG. 3. (Color online) E_C potential profiles of the $In_{0.17}Al_{0.83}N$ (10 nm)/$Al_{0.38}Ga_{0.62}N$ (5 nm)/AlN (0.75 nm)/GaN structure calculated for several $E_{F\ surf}$ positions.

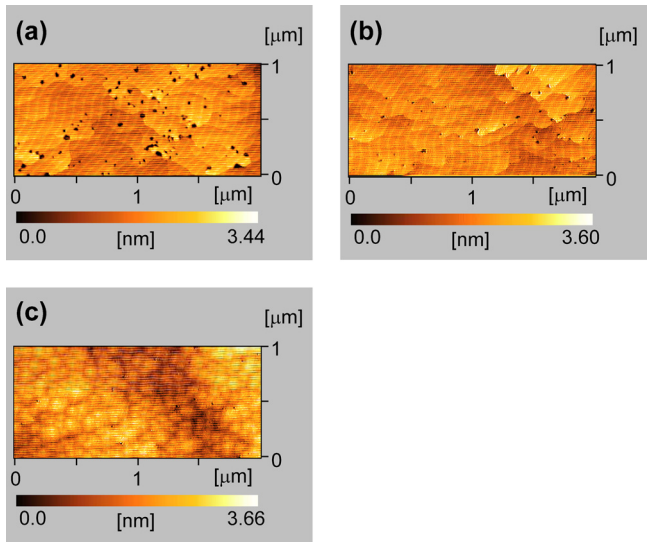

FIG. 4. (Color online) AFM images for (a) $Al_{0.44}Ga_{0.56}N$ (2.0 nm)/GaN, (b) $Al_{0.44}Ga_{0.56}N$ (1.5 nm)/GaN, and (c) $In_{0.18}Al_{0.82}N$ (12 nm)/$Al_{0.44}Ga_{0.56}N$ (1.5 nm)/GaN.

An alternative heterostructure was designed as shown in Fig. 1(b). The Al molar fraction, x, of the $Al_xGa_{1-x}N$ spacer layer was increased to enlarge the band gap. The critical thickness, however, decreases as x increases. The spacer layer should be as thick as possible to obtain a high 2DEG mobility to separate electrons from the bottom of the InAlN layer, even though it should be sufficiently thin to prevent electron accumulation inside the barrier layer. In addition, an excessively high value of x may result in deterioration of the surface flatness. We, therefore, attempted to increase x slightly from $x=0.38$ to 0.44. The corresponding increase in the conduction band offset relative to GaN was estimated to be about 0.1 eV by the calculation described above.

It was expected that the surface flatness of the $InAlN/Al_{0.44}Ga_{0.56}N/GaN$ structure could be superior to that of the conventional InAlN/AlN/GaN structure because the lattice mismatch is reduced. To verify this, the surface morphology of the grown heterostructures was investigated using an atomic force microscope (AFM). The results are summarized in Fig. 4. When the thickness of the $Al_{0.44}Ga_{0.56}N$ layer was greater than 1.5 nm, the number and size of pits increased remarkably as shown in Fig. 4(a) for 2.0 nm thick $Al_{0.44}Ga_{0.56}N$ on GaN. Therefore, the optimal thickness of the $Al_{0.44}Ga_{0.56}N$ layer was determined to be 1.5 nm. The surface morphology of 1.5 nm $Al_{0.44}Ga_{0.56}N$ on GaN shown in Fig. 4(b) was superior to that of an AlN (~1 nm)/GaN surface,[6] which led to a smoother InAlN/AlGaN/GaN surface [root mean square roughness (rms): 0.35 nm], as shown in Fig. 4(c), than that of the conventional InAlN/AlN/GaN (rms: 0.53 nm) structure.[6] The Hall measurement showed that a 2DEG with $n_S=2.1\times10^{13}$ cm^{-2} and $\mu=1100$ $cm^2/V/s$ was obtained for the $In_{0.18}Al_{0.82}N/Al_{0.44}Ga_{0.56}N/GaN$ heterostructure. Although the mobility is lower for the sample with the $Al_{0.44}Ga_{0.56}N$ single spacer layer, it is much higher than the typical value of less than 200 $cm^2/V/s$ for an InAlN/GaN structure without a spacer layer.[4,6]

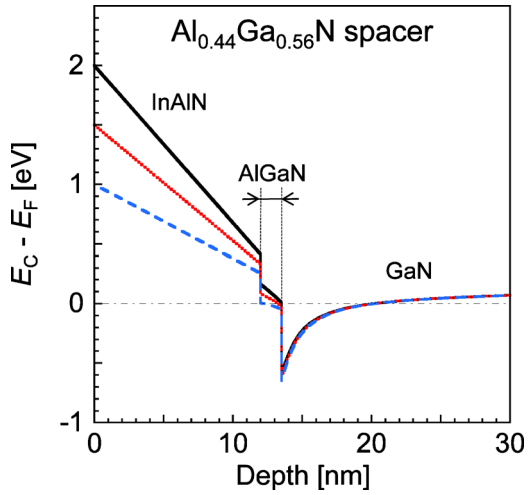

FIG. 5. (Color online) E_C potential profiles of the $In_{0.18}Al_{0.82}N$ (12 nm)/$Al_{0.44}Ga_{0.56}N$ (1.5 nm)/GaN structure calculated for several $E_{F\ surf}$ positions.

A calculation employing the same method used for Fig. 3 showed that InAlN (12 nm)/$Al_{0.44}Ga_{0.56}N$ (1.5 nm) should operate normally as a barrier under positive bias as shown in Fig. 5. Actually, the measured C-V characteristic of the Al_2O_3/$In_{0.18}Al_{0.82}N$/$Al_{0.44}Ga_{0.56}N$/GaN structure exhibited a wide plateau as plotted in Fig. 6. The measured capacitance at approximately −3 V had a value corresponding to the electron accumulation at the $Al_{0.44}Ga_{0.56}N$/GaN interface

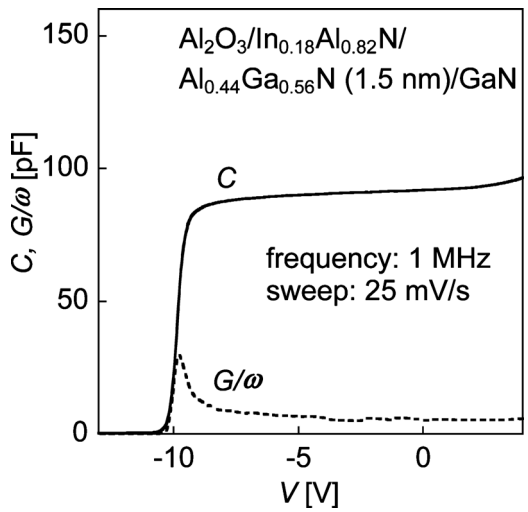

FIG. 6. Measured C-V curve for the Al_2O_3 (13 nm)/$In_{0.18}Al_{0.82}N$ (12 nm)/$Al_{0.44}Ga_{0.56}N$ (1.5 nm)/GaN structure. C_i was estimated to be ~190 pF. The bias voltage was swept from the positive side to the negative side at a sweep rate of 25 mV/s.

and slightly increased as the bias increased toward the onset of electron accumulation at the InAlN surface at approximately 4 V. The positive bias limit of this sample, due to the leakage through the Al_2O_3 layer, was higher than that of the sample with the $Al_{0.38}Ga_{0.62}N$/AlN double spacer layer in Fig. 2. Since the Al_2O_3 layer was as thin as 10 nm, its resistivity should have been affected by the roughness and native oxide components of the InAlN surface before the deposition. The pretreatment, using the BHF solution to remove the SiN_x layer, followed by the sample transfer in air to the ALD chamber was not optimized completely for the InAlN surface, which possibly resulted in the difference of the insulator quality between two samples.

In summary, Al_2O_3 (10 nm)/$In_{0.17}Al_{0.83}N$ (10 nm)/$Al_{0.38}Ga_{0.62}N$ (5 nm)/AlN (0.75 nm)/GaN and Al_2O_3 (13 nm)/$In_{0.18}Al_{0.82}N$ (12 nm)/$Al_{0.44}Ga_{0.56}N$ (1.5 nm)/GaN structures were fabricated and studied. The C-V characteristic of the former structure exhibited an anomalous saturation at a value far below the insulator capacitance under positive bias, indicating electron accumulation at the InAlN/AlGaN interface, while no such saturation was observed in the latter structure. The InAlN/$Al_{0.44}Ga_{0.56}N$ (1.5 nm)/GaN structure showed improved surface flatness compared with the conventional InAlN/AlN/GaN structure. A 2DEG with $n_S=2.1\times10^{13}$ cm^{-2} and $\mu=1100$ $cm^2/V/s$ was obtained by using the $Al_{0.44}Ga_{0.56}N$ single spacer layer. Since thinning the barrier layer is one of the ways of achieving a normally off FET,[5] the InAlN/$Al_{0.44}Ga_{0.56}N$ (1.5 nm)/GaN structure with a thin spacer layer is advantageous from this viewpoint.

[1]O. Ambacher, R. Dimitrov, M. Stutzmann, B. E. Foutz, M. J. Murphy, J. A. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Chumbes, B. Green, A. J. Sierakowski, W. J. Schaff, and L. F. Eastman, Phys. Status Solidi B **216**, 381 (1999).
[2]J. Kuzmík, IEEE Electron Device Lett. **22**, 510 (2001).
[3]M. Higashiwaki and T. Matsui, Jpn. J. Appl. Phys., Part 2 **43**, L768 (2004).
[4]M. Gonschorek, J.-F. Carlin, E. Feltin, M. A. Py, and N. Grandjean, Appl. Phys. Lett. **89**, 062106 (2006).
[5]C. Ostermaier, G. Pozzovivo, J.-F. Carlin, B. Basnar, W. Schrenk, Y. Douvry, C. Gaquière, J.-C. DeJaeger, K. Čičo, K. Fröhlich, M. Gonschorek, N. Grandjean, G. Strasser, D. Pogany, and J. Kuzmík, IEEE Electron Device Lett. **30**, 1030 (2009).
[6]M. Hiroki, N. Maeda, and T. Kobayashi, Appl. Phys. Express **1**, 111102 (2008).
[7]1D Poisson–Schrodinger solver program developed by Prof Gregory Snider, University of Notre Dame, http://www.nd.edu/~gsnider/.
[8]W. Walukiewicz, S. X. Li, J. Wu, K. M. Yu, J. W. Ager III, E. E. Haller, H. Lu, and W. J. Schaff, J. Cryst. Growth **269**, 119 (2004).
[9]R. E. Jones, R. Broesler, K. M. Yu, J. W. Ager III, E. E. Haller, W. Walukiewicz, X. Chen, and W. J. Schaff, J. Appl. Phys. **104**, 123501 (2008).
[10]T. Kubo, H. Taketomi, H. Miyake, K. Hiramatsu, and T. Hashizume, Appl. Phys. Express **3**, 021004 (2010).